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EXAMINER	
CHEN, ALAN S	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,872	WALTON ET AL.	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 11* is/are allowed.

6)☒ Claim(s) *1-6,9,12,13 and 17-21* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Response to Arguments

1. The amendment to the specification has been noted; the objection to the drawings is removed.

2. After further review, the title is considered descriptive; the objection to the title is removed.

3. Applicant amends claim 19 to remove the 35 USC §112 rejection. While the previous reason for the rejection has been rectified, the amendment caused another reason to be made for the same rejection. See the new 35 USC §112 rejection in this Office Action.

4. Applicant's arguments filed 01/25/2006 have been fully considered but they are not persuasive. Applicant makes arguments only pertaining to the prior art reference to Krontz et al. (Krontz), the arguments being summarized below:

A) Krontz does not teach the structure shown in the figure on pg. 11 of remarks.

B) Krontz does not teach each one of electrical contacts of a plurality of printed circuit boards being electrically connected to a corresponding one of the plurality of conductors of the backplane.

C) Prior art does not teach electrically inhibiting the electrical coupling to the electrical component on the additional PCB from the electrical components of the plurality of PCBs.

5. Examiner's response the remarks are given below:

A) It should first be noted that several of the claims ***do not*** require first and second PC boards. Specifically, claims 12-17 and 19-21 ***only*** recite one set of PC boards and do not require, in their claim language, the structure shown on pg. 11 of the remarks. Next, the previous Office Action submitted by the Examiner acknowledges that Krontz does not have a second plurality of printed circuit boards plugged into the backplane. Note that the motherboard in Krontz, Fig. 2, element 206 is construed to be the backplane (IEEE dictionary definition: "(2) A printed circuit board (pcb) on which connectors are mounted, into which boards or plug-in units are inserted", definition attached to this Action). However, Examiner believes a prima facie case of obviousness was established between the Krontz and Locklear et al. (Locklear) reference. Krontz combined with Locklear would indeed disclose a structure similar to that shown in page 11 of applicant's remarks. Locklear clearly discloses two distinct sets of PCBs/slots (Fig. 3, elements 310 and 316 shows faster PCB slots/cards vs. limiting/slower adapter cards). Locklear shows the first and second PCBs are part of the backplane (Fig. 1) and Krontz shows the circuitry for converting being on the backplane as well (Fig. 2, element 208). Applicant does not argue the 35 USC §103 rejection and therefore the rejection is maintained.

B) Examiner does not agree. Fig. 2, element 200 shows multiple slots that represent where printed circuit boards plug in. It is unequivocal that PCBs, particularly using the PCI standard that Krontz discloses ([0023]) have a plurality of electrical contacts resident on *each* PCB that mates with an equal number of electrical contacts on the slot.

C. The amendment by adding "electrically" inhibiting does not narrow the claims down anymore than what was previously presented. While the applicant points to the specification, specifically the SERDES signal, the specification cannot be read into the claims. Physical removal of a circuit card can just as well read on this limitation. Physical removal of a PCB does in fact electrically inhibit all electrical components from communications with the other PCBs. Krontz combined with Locklear disclose this, where Locklear discloses by showing another slot where a limited adapter card can improve speed, where the card can then be physically removed and inserted into the identified slot (Fig. 3, element 316).

Claim Objections

6. Claim 18 objected to because of the following informalities: misspelling of "boards" in lines 3 and 8. Appropriate correction is required.

7. Claim 18 objected to because of the following informalities: last limitation is grammatically awkward. Examiner suggests "electrically inhibiting the electrical coupling to the electrical component...". Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 12,13 and 19-21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claims 12 and 19 recites the limitation "the first plurality of printed circuit boards" in lines 7 and 6-7, respectively. There is insufficient antecedent basis for this limitation in the claim.

11. Claims 20 and 21 are rejected as being dependent on rejected base claim 19.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

ASL 13. Claims ~~12-17~~ 12,13,17 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pat. Pub. No. 2004/0003155 A1 to Krontz.

14. Per Claim 12, Krontz teaches a backplane (Figure 2, element 206, the motherboard meets the definition of "backplane"; IEEE dictionary definition: "(2) A printed circuit board (pcb) on which connectors are mounted, into which boards or plug-in units are inserted", definition attached) having a plurality of conductors (Krontz discloses various versions the PCI standard for the PCBs that go into the expansion slots, paragraph 23, slots each inherently has a plurality of electrical conductors that mates with PCB); a plurality of printed circuit boards plugged into the backplane (see Figure 2, element 200), each one of the printed circuit boards having a plurality of electrical contacts (PCI card inherently has a plurality of contacts that mate with slot

conductors, the plurality of electrical contacts make up the interface for the PCB), each one of the electrical contacts providing an indication of an incapability (see Figure 2, "208", "Slot Speed detector"; [0024] discloses signal from each slot indicates the operating speed of the expansion slots, e.g., what each slot is limited to) of an electrical component on such one of the printed circuit boards (the PCB has a core protocol, e.g., PCI representing the electrical component), each one of such electrical contacts of the plurality of printed circuit boards being electrically connected to a corresponding one of the plurality of conductors of the backplane (PCB electrical contacts mate with slot electrical contracts); and circuitry connected to the plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors (see Figure 2, element 208 and 238; [0025] discloses encoding speed signals, element 210; one embodiment discloses converting speed signals into a serial stream).

15. Per Claim 13, Krontz explicitly discloses the signals as identifying the current operating speed of the expansion slots ([0024]).

16. Per Claim 17, Krontz discloses a method for operating a system (Fig. 5), comprising: providing a backplane system (Fig. 2 shows backplane system) comprising: a plurality of printed circuit boards (Fig. 2, slots 124-136) each one having an electrical component thereon (PCBs use various PCI standards, requiring PCI cores, PCI core construed to be "electrical component"); and a backplane (Fig. 2, element 206, motherboard) having plugged therein the plurality of printed circuit boards (PCBs plugged into slots) for producing a signal indicative of an operating incompatibility of the

electrical components (Fig. 2, element 210 are all the speed ratings of each of the slots, ranges outside of the speed rating are therefore incompatible); interrupting start-up of the system upon detection of such operating incompatibility (Fig. 5, shows startup of system, e.g., system boot; step 504 shows an interruption in the startup process to determine speed slots); and wherein the operating incompatibility is operating protocol (Page 3, [0034] different PCI standards operate at different speeds; "slot speed indicators 402-408 are used to indicate both the current operating speed of the expansion slot 400 and whether the adapter card in the expansion slot is a PCI or PCI-X adapter card").

17. Per Claim 19, this corresponds to the method having the steps for implementing the system disclosed in previous claims (Claim 17). Krontz teaches all the limitations corresponding to the claimed system and therefore teaches the method implementing it.

18. Per Claims 20 and 21, the Krontz et al. reference teaches incompatibility in operating speed and protocol (see Page 3, [0034]; "slot speed indicators 402-408 are used to indicate both the current operating speed of the expansion slot 400 and whether the adapter card in the expansion slot is a PCI or PCI-X adapter card").

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

21. Claims 1-6, 9, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krontz in view of US Pat. Pub. No. 2002/0099875 A1 to Locklear.

22. Per Claim 1, Krontz teaches a backplane (Figure 2, element 206) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, element 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of an incapability (see Figure 2, element 208, "Slot Speed detector"; [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of such electrical contacts of the first plurality of printed circuit boards being electrically connected to a corresponding one of the plurality of conductors of the backplane (Fig. 2, element 200, each slot has electrical contacts that mate with each PCB electrical contact); and circuitry connected to the plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors (see Figure 2, elements 208 and 238; [0012]). Krontz also teaches a decoder, responsive to the logic signals on the plurality of conductors (see Figure 2, element 238; [0026]).

However, Krontz et al. fails to explicitly teach, a *second plurality of printed circuit boards plugged into the backplane selecting an operating characteristic* for electrical components on the second plurality of printed circuit boards, such selected operating characteristic being *compatible with operating characteristics* of the electrical components on the first plurality of printed circuit boards. As for these limitations, Locklear teaches a system in which printed circuit boards (see "adapter cards") select an operating characteristic for electric components being compatible with operating characteristics of the first printed circuit boards (see [0002]), "an architected method exits whereby the I/O bus and adapter card negotiate for the highest supported data transfer rate").

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system supporting compatibility with older adapter cards ("printed circuit boards") that do not support the higher data transfer rates, as taught by Locklear et al. ([0002]). At the time of the invention, it would have also been obvious that the combination of references provided a system visually indicating configuration problems and solutions for I/O buses, as taught by Locklear et al. ([0006]).

23. Per Claim 2, Krontz et al. does not teach selecting the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit boards, as claimed. Locklear teaches a system in which the I/O bus and adapter card "negotiate for the highest supported data transfer rate" ([0002]). At the time of the

invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

24. Per Claim 3, Krontz teaches a backplane (Figure 2, element 206) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, element 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of an incapability (see Figure 2, element 208, "Slot Speed detector"; [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of the first plurality of printed circuit boards being electrically connected to a corresponding one of the plurality of conductors of the backplane (Fig. 2, element 200, each slot has electrical contacts that mate with each PCB electrical contact). Krontz et al. also teaches a decoder, responsive to the logic signals on the plurality of conductors (see Figure 2, element 238; [0026]).

However, Krontz et al. fails to explicitly teach, a *second plurality of printed circuit boards plugged into the backplane selecting an operating characteristic* for electrical components on the second plurality of printed circuit boards, such selected operating characteristic being *compatible with operating characteristics* of the electrical components on the first plurality of printed circuit boards. As for these limitations, Locklear et al. teaches a system in which printed circuit boards (see "adapter cards") select an operating characteristic for electric components being compatible with operating characteristics of the first printed circuit boards ([0002]), "an architected

method exits whereby the I/O bus and adapter card negotiate for the highest supported data transfer rate").

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

25. Per Claim 4, Krontz does not teach selecting the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit boards, as claimed. Locklear teaches a system in which the I/O bus and adapter card "negotiate for the highest supported data transfer rate" ([0002]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

26. Per Claim 5, Krontz teaches a backplane (Figure 2, element 206) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of **speed** incapability (see Figure 2, element 208, "Slot Speed detector"; [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of the first plurality of printed circuit boards being electrically connected to a corresponding one of the plurality of conductors of the backplane (Fig. 2, element 200, each slot has electrical contacts that mate with each PCB electrical contact); and **circuitry** connected to the plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors (see Figure 2, element 208 and 238; [0012]). Krontz also teaches a second

plurality of printed circuit boards plugged into a backplane (see Figure 2, "Backplane"). The reference teaches a decoder, responsive to the logic signals on the plurality of conductors (see Figure 2, element 238; [0026]) which is to be driven by a clock line ([0027]).

However, Krontz fails to explicitly teach, the decoders of the second plurality of printed circuit boards coupled to the electric components thereon the one of the plurality of clock signals having a rate compatible with operating speeds of the electrical components of the first plurality of printed circuit boards, as claimed. As for these limitations, Locklear teaches a system in which printed circuit boards (see "adapter cards") select an operating characteristic for electric components being compatible with operating characteristics of the first printed circuit boards ([0002]), "an architected method exits whereby the I/O bus and adapter card negotiate for the highest supported data transfer rate").

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

27. Per Claim 6, the combination of references teaches circuitry as disclosed in claim 5. However, this is not disclosed as providing a wired-NOR configuration. Nonetheless, Examiner notes that a wired-NOR configuration would have been an obvious example for implementing the circuitry as disclosed by the combination of references as exposed above.

28. Per Claim 9, Krontz does not teach selecting the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit

boards, as claimed. Locklear teaches a system in which the I/O bus and adapter card "negotiate for the highest supported ("compatible") data transfer rate" ([0002]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

29. Per Claim 18, this corresponds to the method having the steps for implementing the system disclosed in previous claims. The combination of references teaches or suggests all the limitations corresponding to the claimed system and therefore teaches the method implementing it.

Allowable Subject Matter

30. Claims 10 and 11 are allowed based on reasons stated in the previous Office Action.

31. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, based on reasons stated in the previous Office Action.

Conclusion

32. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
04/17/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
4/29/06